

Zilog

AC and DC Characteristics

Preliminary

September 1982

The Zilog logo is a large, bold, black graphic that fills the entire frame. It is composed of the letters 'Z', 'i', 'l', 'o', and 'g' in a stylized, blocky font. The 'Z' is particularly large and prominent on the left side. The 'i' and 'l' are smaller and positioned to the right of the 'Z'. The 'o' and 'g' are also large and positioned to the right of the 'l'. The letters are all in a solid black color and are set against a white background. The overall effect is a high-contrast, minimalist design.

ESOL Low Power Peripherals PIO, CTC, and SIO

AC and DC Characteristics



February

ESOL LOW POWER PERIPHERALS
PIO, CTC, AND SIO

September 1982

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Absolute Maximum Ratings

Voltages on all inputs and outputs
with respect to GND -0.3 V to +7.0 V

As Specified in
Operating Ambient Ordering Information
Temperature in Product Specifications
Storage Temperature -65°C to +150°C

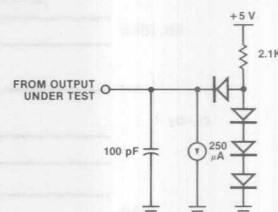
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Test Conditions

The characteristics below apply for the following test conditions, unless otherwise noted. All voltages are referenced to GND (0 V). Positive current flows into the referenced pin. Available operating temperature range is:

■ $S^* = 0^\circ\text{C to } +70^\circ\text{C},$
 $+4.75\text{ V} \leq V_{CC} \leq +5.25\text{ V}$

*See Ordering Information section in product specifications for package temperature range and product number.



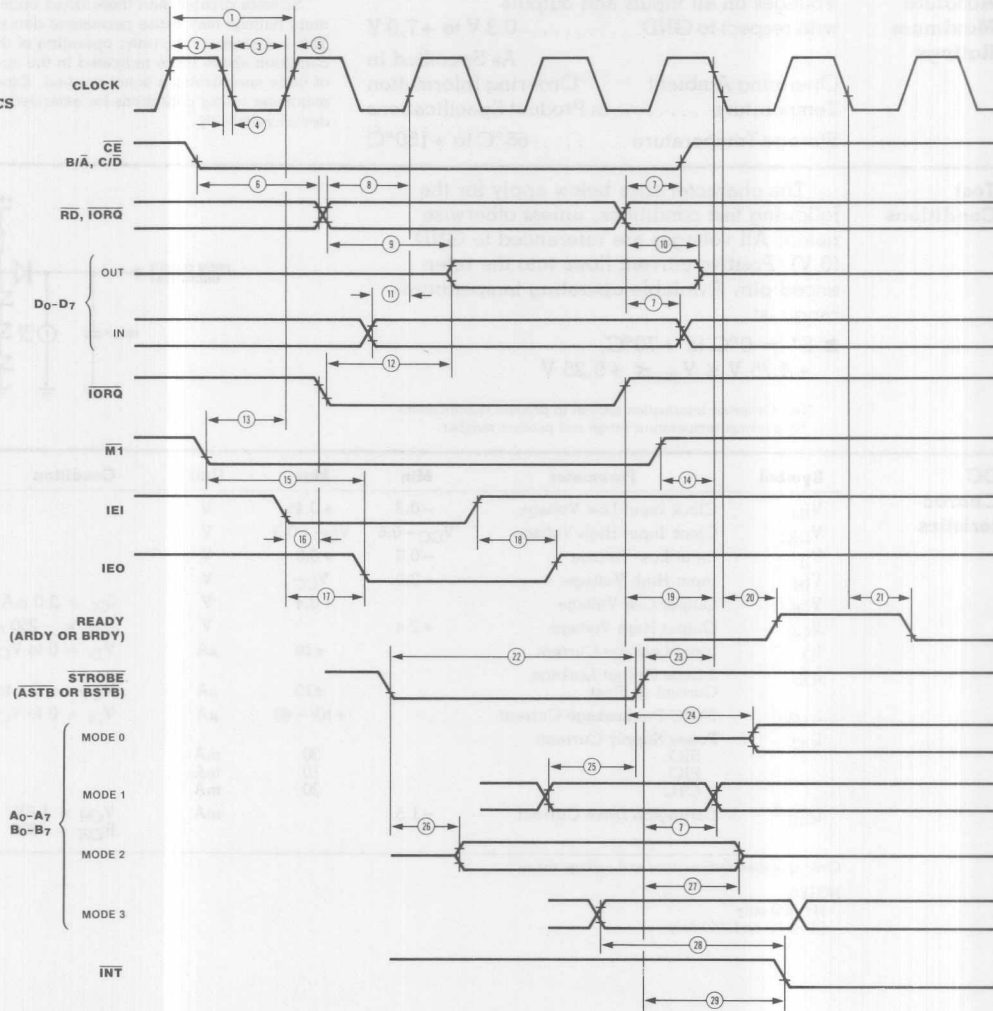
DC Charac- teristics	Symbol	Parameter	Min	Max	Unit	Condition
	V_{ILC}	Clock Input Low Voltage	-0.3	+0.45	V	
	V_{IHC}	Clock Input High Voltage	$V_{CC} - 0.6$	$V_{CC} + 0.3$	V	
	V_{IL}	Input Low Voltage	-0.3	+0.8	V	
	V_{IH}	Input High Voltage	+2.0	V_{CC}	V	
	V_{OL}	Output Low Voltage		+0.4	V	$I_{OL} = 2.0\text{ mA}$
	V_{OH}	Output High Voltage	+2.4		V	$I_{OH} = -250\text{ }\mu\text{A}$
	I_{LI}	Input Leakage Current		± 10	μA	$V_{IN} = 0\text{ to } V_{CC}$
	I_{OL}	3-State Output Leakage Current in Float		± 10	μA	$V_{OUT} = 0.4\text{ to } V_{CC}$
	$I_{L(SY)}^1$	SYNC Pin Leakage Current		+10/-40	μA	$V_{IN} = 0\text{ to } V_{CC}$
	I_{CC}	Power Supply Current:				
		SIO		30	mA	
		PIO		10	mA	
		CTC		20	mA	
	I_{OHD}^2	Darlington Drive Current	-1.5		mA	$V_{OH} = 1.5\text{ V}$ $R_{EXT} = 390\Omega$

Over specified temperature and voltage range.

NOTES:

- [1] SIO only
- [2] CTC and PIO only

**Z8320-1 and
Z8320-3
Z80L PIO
AC
Characteristics**



**Z8320-1 and
Z8320-3
Z80L PIO**

AC

Characteristics
(Continued)

Number	Symbol	Parameter	Z8320-1 (1.0 MHz)		Z8320-3 (2.5 MHz)		Notes*
			Min	Max	Min	Max	
1	TcC	Clock Cycle Time	1000		400		[1]
2	TwCH	Clock Width (High)	470	2000	170	2000	
3	TwCl	Clock Width (Low)	470	2000	170	2000	
4	TfC	Clock Fall Time		30		30	
5	TrC	Clock Rise Time		30		30	
6	TsCS(RI)	$\overline{CE}$, B/ $\overline{A}$, C/ $\overline{D}$ to $\overline{RD}$, $\overline{IORQ}$ $\downarrow$ Setup Time	140		50		[6]
7	Th	Any Hold Times for Specified Setup Time	0		0		
8	TsRI(C)	$\overline{RD}$, $\overline{IORQ}$ to Clock $\uparrow$ Setup Time	300		115		
9	TdRI(DO)	$\overline{RD}$, $\overline{IORQ}$ $\downarrow$ to Data Out Delay	1090		430		[2]
10	TdRI(DOs)	$\overline{RD}$, $\overline{IORQ}$ $\downarrow$ to Data Out Float Delay		410		160	
11	TsDI(C)	Data In to Clock $\uparrow$ Setup Time	140		50		CL = 50 pF
12	TdIO(DOI)	$\overline{IORQ}$ $\downarrow$ to Data Out Delay (INTACK Cycle)		860		340	[3]
13	TsM1(Cr)	$\overline{M1}$ $\downarrow$ to Clock $\uparrow$ Setup Time	540		210		
14	TsM1(Cf)	$\overline{M1}$ $\uparrow$ to Clock $\downarrow$ Setup Time (M1 Cycle)	0		0		[8]
15	TdM1(IEO)	$\overline{M1}$ $\downarrow$ to IEO $\downarrow$ Delay (Interrupt Immediately Preceding M1 $\downarrow$)		760		300	[5, 7]
16	TsIEI(IO)	IEI to $\overline{IORQ}$ $\downarrow$ Setup Time (INTACK Cycle)	360		140		[7]
17	TdIEI(IEOf)	IEI $\downarrow$ to IEO $\downarrow$ Delay		480		190	[5] CL = 50 pF
18	TdIEI(IEOr)	IEI $\uparrow$ to IEO $\uparrow$ Delay (after ED Decode)		540		210	[5]
19	TcIO(C)	$\overline{IORQ}$ $\uparrow$ to Clock $\downarrow$ Setup Time (To Activate READY on Next Clock Cycle)	560		220		
20	TdC(RDYr)	Clock $\downarrow$ to READY $\uparrow$ Delay	510		200		[5] CL = 50 pF
21	TdC(RDYf)	Clock $\downarrow$ to READY $\uparrow$ Delay	390		150		[5]
22	TwSTB	$\overline{STROBE}$ Pulse Width	390		150		[4]
23	TsSTB(C)	$\overline{STROBE}$ $\uparrow$ to Clock $\downarrow$ Setup Time (To Activate READY on Next Clock Cycle)	560		220		[5]
24	TdIO(PD)	$\overline{IORQ}$ $\uparrow$ to PORT DATA Stable Delay (Mode 0)		510		200	[5]
25	TsPD(STB)	PORT DATA to $\overline{STROBE}$ $\uparrow$ Setup Time (Mode 1)	660		260		
26	TdSTB(PD)	$\overline{STROBE}$ $\downarrow$ to PORT DATA Stable (Mode 2)		590		230	[5]
27	TdSTB(PDr)	$\overline{STROBE}$ $\uparrow$ to PORT DATA Float Delay (Mode 2)		510		200	CL = 50 pF
28	TdPD(INT)	PORT DATA Match to $\overline{INT}$ $\downarrow$ Delay (Mode 3)		1360		540	
29	TdSTB(INT)	$\overline{STROBE}$ $\uparrow$ to $\overline{INT}$ $\downarrow$ Delay		1240		490	

NOTES:

- [1] TcC = TwCh + TwCl + TrC + TfC.
- [2] Increase TdRI(DO) by 10 ns for each 50 pF increase in load up to 200 pF max.
- [3] Increase TdIO(DOI) by 10 ns for each 50 pF, increase in loading up to 200 pF max.
- [4] For Mode 2: TwSTB > TsPD(STB).
- [5] Increase these values by 2 ns for each 10 pF increase in loading up to 100 pF max.

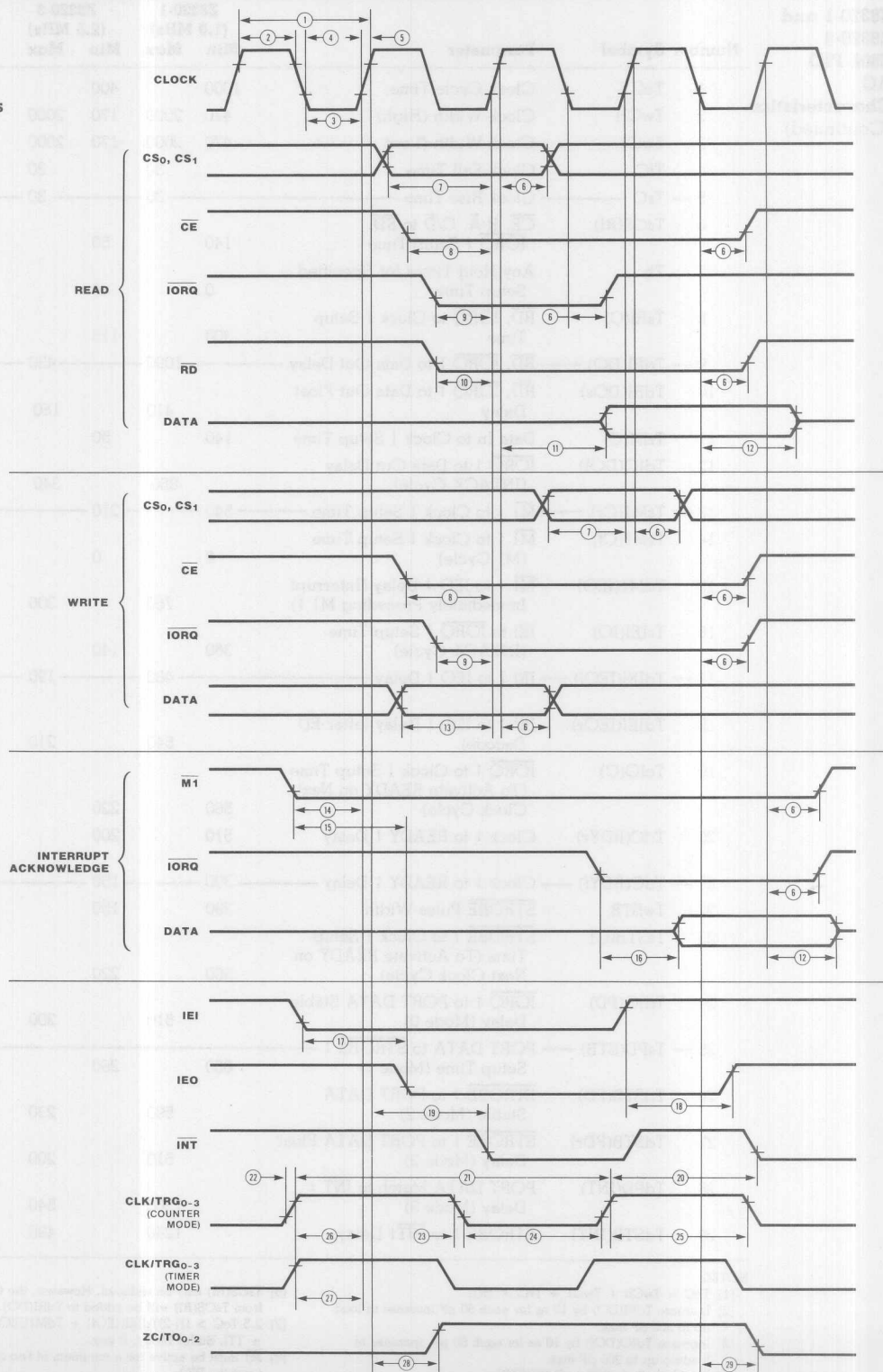
[6] TsCS(RI) may be reduced. However, the time subtracted from TsCS(RI) will be added to TdRI(DO).

[7] $2.5 \text{ TcC} > (N-2) \text{ TdIEI(IEOf)} + \text{TdM1(IEO)} + \text{TsIEI(IO)} \pm \text{TTL Buffer Delay}$, if any.

[8] $\overline{M1}$ must be active for a minimum of two clock cycles to reset the PIO.

* Timings are preliminary and subject to change.

Z8330-1 and
Z8330-3
Z80L CTC
AC
Characteristics



**Z8330-1 and
Z8330-3
Z80L CTC**

AC

Characteristics

(Continued)

Number	Symbol	Parameter	Z8330-1 (1.0 MHz)		Z8330-3 (2.5 MHz)		Notes†*
			Min	Max	Min	Max	
1	TcC	Clock Cycle Time	1000		400		
2	TwCH	Clock Width (High)	470		170		
3	TwCl	Clock Width (Low)	470	2000	170	2000	
4	TfC	Clock Fall Time		30		30	
5	TrC	Clock Rise Time		30		30	
6	Th	All Hold Times	0		0		
7	TsCS(C)	CS to Clock ↑ Setup Time	640		250		
8	TsCE(C)	$\overline{CE}$ to Clock ↑ Setup Time	510		200		
9	TsIO(C)	$\overline{IORQ}$ ↓ to Clock ↑ Setup Time	640		250		
10	TsRD(C)	$\overline{RD}$ ↓ to Clock ↑ Setup Time	610		240		
11	TdC(DO)	Clock ↑ to Data Out Delay		610		240	[2]
12	TdC(DOz)	Clock ↑ to Data Out Float Delay		590		230	
13	TsDI(C)	Data In to Clock ↑ Setup Time	160		60		
14	TsM1(C)	M1 to Clock ↑ Setup Time	540		210		
15	TdM1(IEO)	M1 ↑ to IEO ↓ Delay (Interrupt immediately preceding M1)		760		300	[3]
16	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay (INTA Cycle)		860		340	[2]
17	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		490		190	[3]
18	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (After ED Decode)		560		220	[3]
19	TdC(INT)	Clock ↑ to $\overline{INT}$ ↓ Delay		((1) + 510)		((1) + 200)	[4]
20	TdCLK(INT)	CLK/TRG ↑ to $\overline{INT}$ ↓ tsCTR(C) satisfied		((19) + (26))		((19) + (26))	[5]
		tsCTR(C) not satisfied		((1) + (19) + (26))		((1) + (19) + (26))	[5]
21	TcCTR	CLK/TRG Cycle Time		2TcC		2TcC	[5]
22	TrCTR	CLK/TRG Rise Time		50		50	
23	TfCTR	CLK/TRG Fall Time		50		50	
24	TwCTRL	CLK/TRG Width (Low)	510		200		
25	TwCTRh	CLK/TRG Width (High)	510		200		
26	TsCTR(Cs)	CLK/TRG ↑ to Clock ↑ Setup Time for Immediate Count	760		300		[5]
27	TsCTR(Ct)	CLK/TRG ↑ to Clock ↑ Setup Time for enabling of Prescaler on following clock↑	540		210		[4]
28	TdC(ZC/TOr)	Clock ↑ to ZC/TO ↑ Delay		660		260	
29	TdC(ZC/TOf)	Clock ↓ to ZC/TO ↓ Delay		490		190	

NOTES:

[1] $TcC = TwCh + TwCl + TrC + TfC$.

[2] Increase delay by 10 ns for each 50 pF increase in loading, 200 pF maximum for data lines, and 100 pF for control lines.

[3] Increase delay by 2 ns for each 10 pF increase in loading, 100 pF maximum.

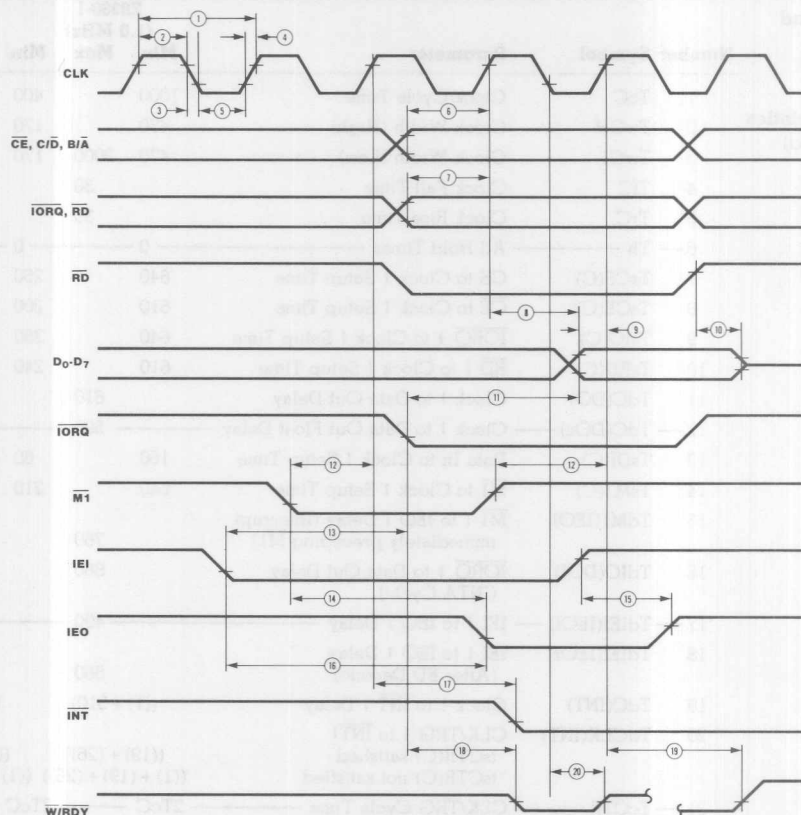
[4] Timer mode.

[5] Counter mode.

* $\overline{RESET}$ must be active for a minimum of 3 clock cycles.

† Units are nanoseconds unless otherwise specified; parenthetical numbers reference the table number of a parameter, e.g., (1) refers to TcC; timings are preliminary and subject to change.

**Z8340-1 and
Z8340-3
Z80L SIO
AC
Characteristics**



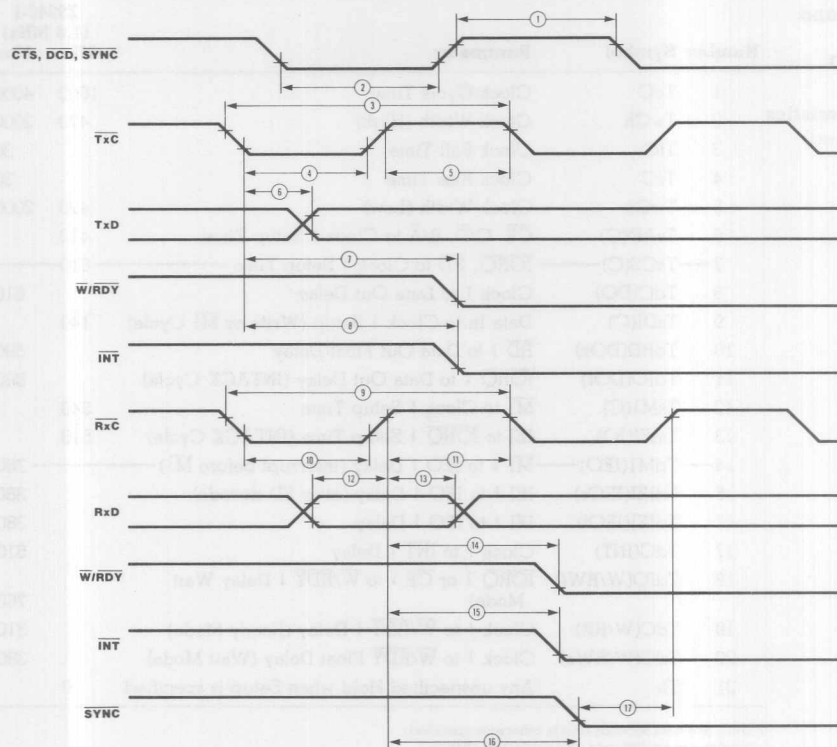
**Z8340-1 and
Z8340-3
Z80L SIO**

**AC
Characteristics
(Continued)**

Number	Symbol	Parameter	Z8340-1 (1.0 MHz)		Z8340-3 (2.5 MHz)		Notes†
			Min	Max	Min	Max	
1	TcC	Clock Cycle Time	1000	4000	400	4000	
2	TwCh	Clock Width (High)	470	2000	170	2000	
3	TfC	Clock Fall Time		30		30	
4	TrC	Clock Rise Time		30		30	
5	TwCl	Clock Width (Low)	470	2000	170	2000	
6	TsAD(C)	$\overline{CE}$, C/ $\overline{D}$, B/ $\overline{A}$ to Clock ↑ Setup Time	410		160		
7	TsCS(C)	$\overline{IORQ}$, $\overline{RD}$ to Clock ↑ Setup Time	610		240		
8	TdC(DO)	Clock ↑ to Data Out Delay		610		240	
9	TsDI(C)	Data In to Clock ↑ Setup (Write or $\overline{M1}$ Cycle)	140		50		
10	TdRD(DOz)	$\overline{RD}$ ↑ to Data Out Float Delay		590		230	
11	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay (INTACK Cycle)		860		340	
12	TsM1(C)	$\overline{M1}$ to Clock ↑ Setup Time	540		210		
13	TsIEI(IO)	IEI to $\overline{IORQ}$ ↓ Setup Time (INTACK Cycle)	510		200		
14	TdM1(IEO)	$\overline{M1}$ ↑ to IEO ↓ Delay (interrupt before $\overline{M1}$)		760		300	
15	TdIEI(IEOr)	IEI ↑ to IEO ↓ Delay (after ED decode)		380		150	
16	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		380		150	
17	TdC(INT)	Clock ↑ to $\overline{INT}$ ↓ Delay		510		200	
18	TdIO(W/RWf)	$\overline{IORQ}$ ↓ or $\overline{CE}$ ↓ to $\overline{WRDY}$ ↓ Delay (Wait Mode)		760		300	
19	TdC(W/RR)	Clock ↑ to $\overline{WRDY}$ ↓ Delay (Ready Mode)		310		120	
20	TdC(W/RWz)	Clock ↑ to $\overline{WRDY}$ Float Delay (Wait Mode)		390		150	
21	Th	Any unspecified Hold when Setup is specified	0		0		

† Units are nanoseconds unless otherwise specified;
timings are preliminary and subject to change.

**Z8340-1 and
Z8340-3
Z80L SIO
AC
Characteristics
(Continued)**



Number	Symbol	Parameter	Z8340-1 (1.0 MHz)		Z8340-3 (2.5 MHz)		Notes†
			Min	Max	Min	Max	
1	TwPh	Pulse Width (High)	500		200		
2	TwPl	Pulse Width (Low)	500		200		
3	TcTx̄C	Tx̄C Cycle Time	1000	∞	400	∞	
4	TwTx̄C1	Tx̄C Width (Low)	460	∞	180	∞	
5	TwTx̄Cch	Tx̄C Width (High)	460	∞	180	∞	
6	TdTx̄C(TxD)	Tx̄C ↓ to Tx̄D Delay (x1 Mode)		1000		400	
7	TdTx̄C(W/RRf)	Tx̄C ↓ to W/RDY ↓ Delay (Ready Mode)	5	9	5	9	Clk Periods*
8	TdTx̄C(INT)	Tx̄C ↓ to INT ↓ Delay	5	9	5	9	Clk Periods*
9	TcRx̄C	Rx̄C Cycle Time	1000	∞	400	∞	
10	TwRx̄C1	Rx̄C Width (Low)	460	∞	180	∞	
11	TwRx̄Cch	Rx̄C Width (High)	460	∞	180	∞	
12	TsRx̄D(RxC)	RxD to Rx̄C ↑ Setup Time (x1 Mode)	0		0		
13	ThRx̄D(RxC)	Rx̄C ↑ to Rx̄D Hold Time (x1 Mode)	360		140		
14	TdRx̄C(W/RRf)	Rx̄C ↑ to W/RDY ↓ Delay (Ready Mode)	10	13	10	13	Clk Periods*
15	TdRx̄C(INT)	Rx̄C ↑ to INT ↓ Delay	10	13	10	13	Clk Periods*
16	TdRx̄C(SYNC)	Rx̄C ↑ to SYNC ↓ Delay (Output Modes)	4	7	4	7	Clk Periods*
17	TsSYNC(RxC)	SYNC ↓ to Rx̄C ↑ Setup (External Sync Modes)	-100		-100		

In all modes, the System Clock rate must be at least five times the maximum data rate.
RESET must be active a minimum of one complete Clock Cycle.

* System Clock

† Units are nanoseconds unless otherwise specified; timings are preliminary and subject to change.